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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/708,450	11/09/2000	YOSHITAKA NAKAMURA	501.39149X00	2432

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EXAMINER
OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/708,450	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *1-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the invention of group II, claims 20-33 in Paper No. 6 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the third and fourth metal layer that is part of the second metal layer, as required in claim 31, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: in line 13 of page 17, "high" should be replaced with "higher'.

Appropriate correction is required.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 20-33 are objected to because of the following informalities:

in line 7 of claim 20, "boring" should be replaced with "etching";

in line 17, of claim 20 "electrode" should be replaced with "electrodes" ***or*** "a" should be inserted between "forming" and "columnar" in lines 10 and 11 and "electrodes" should be replaced with "electrode" in line 11;

in line 8 of claim 26, "continuously" should be replaced with "continuous"; and

in line 8 of claim 29, "continuously" should be replaced with "continuous".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 31 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no disclosure of a method, wherein the second metal layer of the second electrode comprises a third metal layer formed by sputtering and a fourth metal layer formed by CVD.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 20-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites the limitation "...a metal compound for burying the inside of said holes..." in lines 10 and 11. The scope of the claim is vague, because it is not understood how the metal compound can bury the inside of the holes.

Claim 21 recites the limitations, "...said second layer is etched..." and "...said first layer is etched..." in lines 3 and 4 respectively. The scope of the claim is not clear because it is not possible to discern which first and second layer is being referenced.

Claim 29 recites the limitation, "...second electrodes with respect to a plurality of said first electrodes..." in lines 8 and 9. The scope of the claim is not clear because it seems to imply that the second electrode being continuous is reliant on the first electrodes. It is not understood how this is so.

Claim 29 recites the limitation, "...as to bury the spaces between said mutually..." in lines 14 and 15. The scope of the claim is vague because it is not known what is meant by burying spaces, or how spaces can be buried.

Claim 31 recites the limitation, "...second metal layer comprises a third metal layer...and a fourth metal layer...". The scope of the claim is nebulous because it is not understood how a second metal layer can include a third and fourth metal layer. This would require the third metal layer to also be the second metal layer and the fourth metal layer would have to also be the second metal layer.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 20-26, 30, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,837,578 to Fan et al. in view of US patent No. 5,854,104 to Onishi et al.

Regarding claim 20, Fan et al. teaches a method of manufacturing an integrated circuit, comprising the steps of:

forming a C.O.B. structure (Col. 3, lines 20-23), which would have inherently required forming bit lines and contacts in a first insulating film;

forming a second interlayer insulating film (33) and electrode-forming insulating film (36);

etching holes in the electrode-forming insulating film (Fig. 3(e));

forming a conductive film (39) in the holes, and removing the electrode-forming insulating film to form cylindrical capacitor first electrodes (Fig. 3(h));

depositing a ferroelectric capacitor dielectric film (310) over the first electrodes; and

depositing and patterning a first a conductor layer (311) to form a second electrode.

Fan et al. does not teach forming a metal or metal compound for forming the lower electrode. Fan et al. does not teach patterning first and second conductor layers to form second electrodes. Fan et al. does not teach depositing a third interlayer insulating film to cover the second electrodes, and forming connection holes reaching the second electrodes and the first layer wiring.

Onishi et al. teaches using a metal to form the lower electrode (13) of a ferroelectric capacitor, patterning first (15) and second (16) conductor layers to form second electrodes and forming a third insulating film (18) and forming a connection hole to the second electrode (Col. 7, lines 38-43).

It would have been obvious to one of ordinary skill in the art to incorporate the platinum electrode used by Onishi et al. into the method of making an integrated circuit taught by Fan et al. since platinum is desirable for use as electrode material in ferroelectric capacitors due to the resistance it has to oxidation. If an oxide forms on the electrode layer, it would result in a low-k dielectric forming between the ferroelectric layer and the electrode and a reduction of capacitance. It would have further been obvious to one of ordinary skill in the art to form the second conductive layer, which prevents diffusion, since it is desirable to prevent unwanted diffusion of metals. It is also desirable to form a connection to the capacitor to give it functionality in the integrated circuit. Since etching is a well known method of forming contact holes in insulation film, it would have been a matter of obvious design choice to employ this technique.

Neither Fan et al. nor Onishi et al. teach etching second holes in the third interlayer insulating film that extend through to the first layer wiring. It would have been obvious to one of ordinary skill in the art to form connection holes to the first layer wiring since it is desirable to manufacture functional devices.

Regarding claim 21, Fan et al. does not teach using the second layer of the second electrode as a mask to form the first layer of the second electrode. Onishi et al.

teaches a method wherein the second layer of the second electrode masks the first layer of the second electrode as it is etched. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Onishi et al. into the method taught by Fan et al. for reasons discussed above.

Regarding claims 22, 26 and 32, Fan et al. teaches a method of making an integrated circuit, comprising the steps of:

forming first electrodes on a first insulating film;

forming a capacitor dielectric film over the first electrode; and

forming second electrodes over the capacitor dielectric film.

Fan et al. does not teach forming a second insulating film over the second electrodes, wherein the film has an opening for exposing a part of the second electrodes. Fan et al. does not teach a method wherein the formation of the second electrode includes forming a first metal layer by CVD. Fan et al. does not teach a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over the first metal layer.

Onishi et al. teaches forming a second insulating film over the second electrode having an opening for exposing a part of the second electrodes. Onishi et al. teaches a method wherein forming the second electrode includes depositing a platinum layer by a known method (Col. 5, lines 12 and 13). Onishi et al. teaches a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over the first metal layer. It would have been obvious to one of ordinary skill in the art to form the opening in the second insulating film since it is desirable to form a

connection to the capacitor to give it functionality in the integrated circuit. It would have further been obvious to provide a conductor layer in the opening since it is needed to provide a connection. It would have been obvious to use CVD to deposit the metal as a matter of obvious design choice. It would have been further obvious to incorporate the method taught by Onishi et al. into the method taught by Fan et al. for reasons discussed above.

Neither Fan et al. nor. Onishi et al. teach a method of making an integrated circuit, wherein the second metal layer is thicker than the first metal layer. It is known in the art to vary the thickness of capacitor electrode layers to achieve desired performance characteristics as well as structural integrity. It would have been a matter of obviousness to find the optimal thickness of the second metal layer through routine experimentation.

Regarding claim 23, Fan et al. does not teach a method of making an integrated circuit, wherein the first metal layer is platinum or ruthenium. Onishi et al. teaches using platinum for the first metal layer (13) of a ferroelectric capacitor. It would have been obvious to one of ordinary skill in the art to incorporate the platinum electrode used by Onishi et al. into the method of making an integrated circuit taught by Fan et al. since platinum is desirable for use as electrode material in ferroelectric capacitors due to the resistance it has to oxidation.

Regarding claims 24 and 33, Fan et al. does not teach a method, wherein the second metal layer comprises tungsten or tungsten nitride. Onishi et al. teaches a method, wherein the second metal layer comprises titanium nitride. It would have been

obvious to one of ordinary skill in the art to substitute titanium nitride with tungsten nitride since the two refractory metals have similar properties.

Regarding claims 25 and 30, Fan et al. does not teach a method of making an integrated circuit, wherein the second metal layer is formed by sputtering. Onishi et al. teaches a method of making an integrated circuit, wherein the second metal layer is formed by sputtering (Col. 5, lines 9-14). It would have been obvious to incorporate the teaching of Onishi et al. into the teaching of Fan et al. for reasons discussed above.

Regarding claim 29, Fan et al. teaches a method of making an integrated circuit, including the steps of:

forming a first electrode over a first insulating film;

forming a capacitor dielectric over the first electrode; and

forming a second electrode over the capacitor dielectric.

Fan et al. does not teach a method of making an integrated circuit, wherein the formation step of the second electrode includes forming a first metal layer and a second metal layer. Onishi et al. teaches a method of making an integrated circuit, wherein the formation step of the second electrode includes forming a first metal layer and a second metal layer. It would have been obvious incorporate the teaching of Onishi et al. into the method taught by Fan et al. for reasons discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

DWO
March 7, 2002

TOM THOMAS
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